CLAIMS:

What is claimed is:

1. A dual deadtime pulse width modulation generator for a processor comprising:

deadtime generation circuitry operable to generate a first pulse width modulated signal and a second pulse width modulated signal complementary to the first pulse width modulated signal, wherein there is a first delay between inactivation of the first pulse width modulated signal and activation of the second pulse width modulated signal, a second delay between inactivation of the second pulse width modulated signal and activation of the first pulse width modulated signal, and the first and second delays are not equal.

2. The dual deadtime pulse width modulation generator of claim 1, wherein the first delay and the second delay are independently settable.

3. A dual deadtime pulse width modulation generator for a processor comprising:

pulse width modulation generation circuitry operable to generate a first pulse width modulated signal; and

deadtime generation circuitry comprising:

first circuitry operable to generate a second pulse width modulated signal from the first pulse width modulated signal and a third pulse width modulated signal from the first pulse width modulated signal, the third pulse width modulated signal complementary to the second pulse width modulated signal, and

second circuitry operable to generate a first delay between inactivation of the second pulse width modulated signal and activation of the third pulse width modulated

signal and a second delay between inactivation of the third pulse width modulated signal and activation of the second pulse width modulated signal, wherein the first and second delays are not equal.

4. The dual deadtime pulse width modulation generator of claim 3, wherein the second circuitry comprises a first register operable to store a value for setting the first delay and a second register operable to store a value for setting the second delay.

5. The dual deadtime pulse width modulation generator of claim 4, wherein the second circuitry further comprises a first edge detector operable to detect a first edge of the first pulse width modulated signal and initiate generation of the first delay and a second edge detector operable to detect a second edge of the first pulse width modulated signal and initiate generation of the second delay.

6. The dual deadtime pulse width modulation generator of claim 5, wherein the deadtime generation circuitry further comprises third circuitry operable to generate a first clock signal that is input to the second circuitry for generating the first and second delays.

7. The dual deadtime pulse width modulation generator of claim 6, wherein the third circuitry comprises a prescaler operable to generate the first clock signal by prescaling a second clock signal.

8. The dual deadtime pulse width modulation generator of claim 7, wherein the third circuitry further comprises circuitry operable to set the prescaler to a first prescale setting to generate the first clock signal for generating the first delay and to set the prescaler to a second prescale setting to generate the first clock signal for generating the second delay.

9. A processor comprising:

deadtime generation circuitry operable to generate a first pulse width modulated signal and a second pulse width modulated signal complementary to the first pulse width modulated signal, wherein there is a first delay between inactivation of the first pulse width modulated signal and activation of the second pulse width modulated signal, a second delay between inactivation of the second pulse width modulated signal and activation of the first pulse width modulated signal, and the first and second delays are not equal.

10. The processor of claim 9, wherein the first delay and the second delay are independently settable.

11. A processor comprising:

pulse width modulation generation circuitry operable to generate a first pulse width modulated signal; and

deadtime generation circuitry comprising:

first circuitry operable to generate a second pulse width modulated signal from the first pulse width modulated signal and a third pulse width modulated signal from the first

pulse width modulated signal, the third pulse width modulated signal complementary to the second pulse width modulated signal, and

second circuitry operable to generate a first delay between inactivation of the second pulse width modulated signal and activation of the third pulse width modulated signal and a second delay between inactivation of the third pulse width modulated signal and activation of the second pulse width modulated signal, wherein the first and second delays are not equal.

12. The processor of claim 11, wherein the second circuitry comprises a first register operable to store a value for setting the first delay and a second register operable to store a value for setting the second delay.

13. The processor of claim 12, wherein the second circuitry further comprises a first edge detector operable to detect a first edge of the first pulse width modulated signal and initiate generation of the first delay and a second edge detector operable to detect a second edge of the first pulse width modulated signal and initiate generation of the second delay.

14. The processor of claim 13, wherein the deadtime generation circuitry further comprises third circuitry operable to generate a first clock signal that is input to the second circuitry for generating the first and second delays.

15. The processor of claim 14, wherein the third circuitry comprises a prescaler operable to generate the first clock signal by prescaling a second clock signal.

16. The processor of claim 15, wherein the third circuitry further comprises circuitry operable to set the prescaler to a first prescale setting to generate the first clock signal for generating the first delay and to set the prescaler to a second prescale setting to generate the first clock signal for generating the second delay.